Overview of Modifications to the CHARA Array Delay Lines

Nils Turner

29 April 2025 / CHARA Winter/Spring Meeting, Nice

Overview

- The Problem

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- Embedded Metrology Box

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- OPLE “glitches”

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- Future work

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  - Took 5 months to assemble

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- There is a second servo cycle that runs every 1 msec which is used for fringe tracking

Embedded Metrology Box

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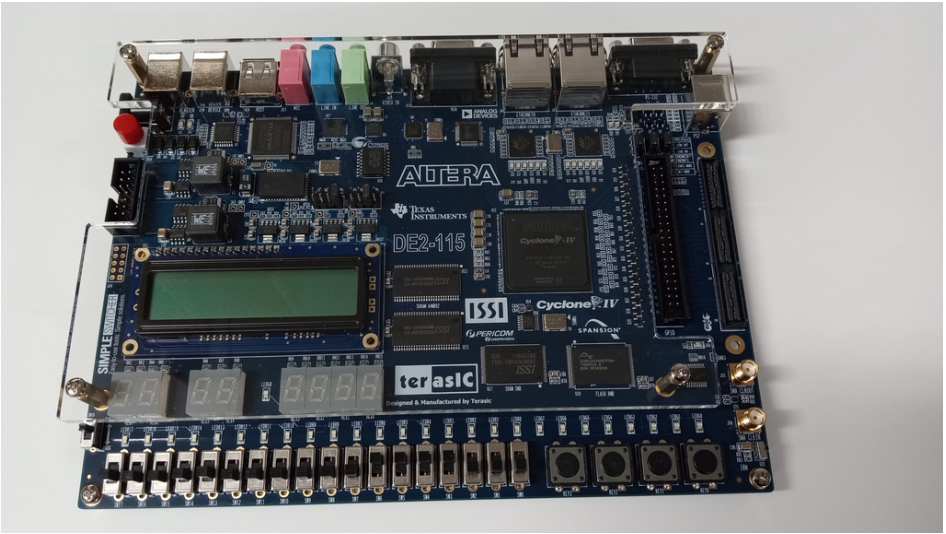
Embedded Metrology Box



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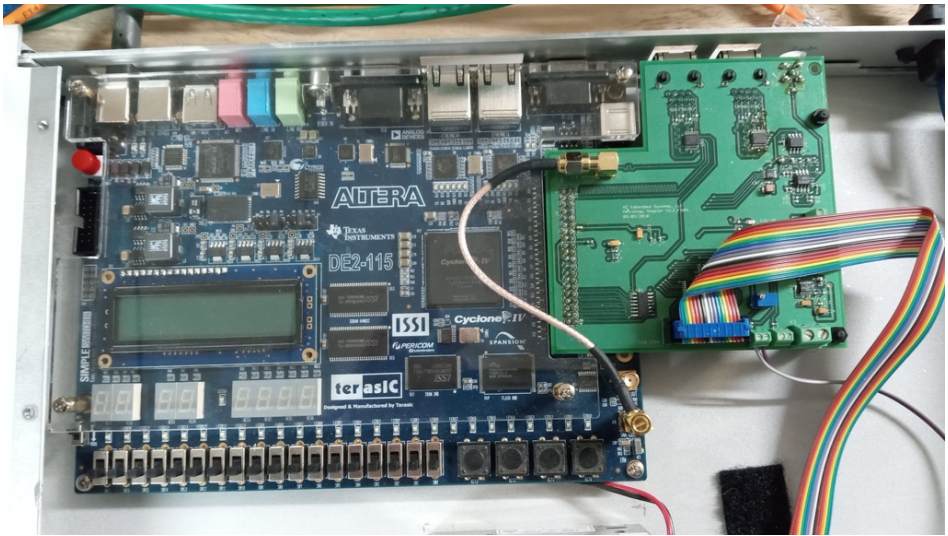

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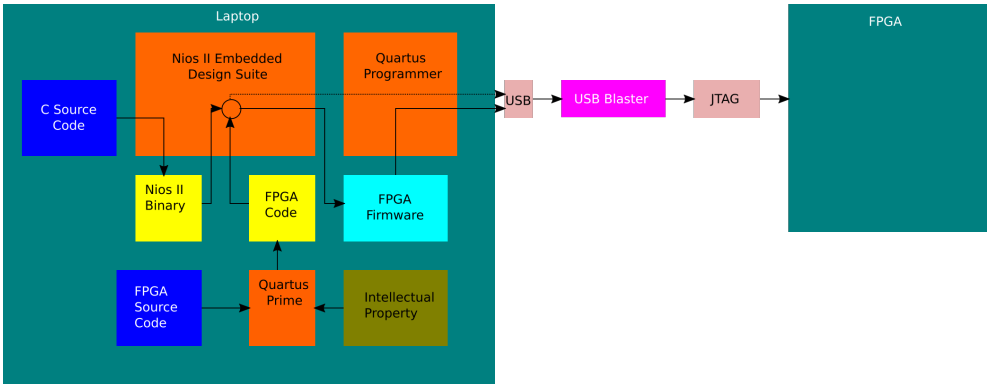
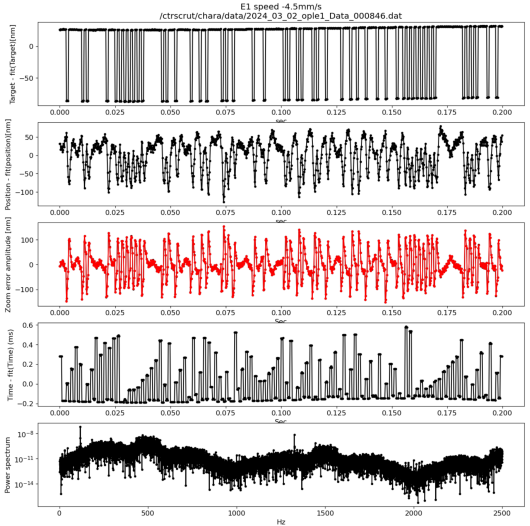


FPGA Programming Flow Chart

OPLE “glitches”



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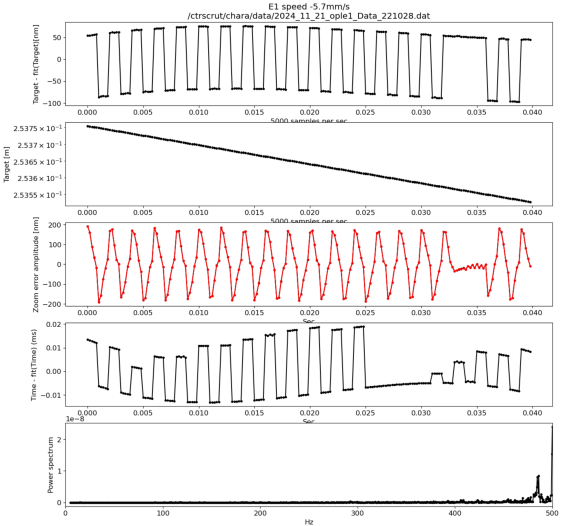

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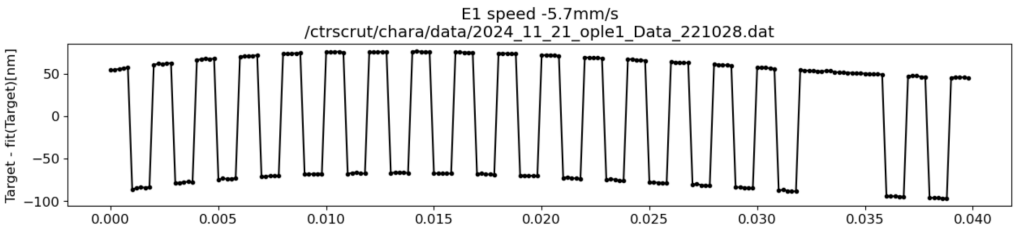

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- Each interrupt that occurs at a 1 msec boundary is used to time tag the target data point
- The target position is interpolated between the 1 msec boundaries to match the 200 μsec telemetry cycle
- If the clock happens to jitter more than 25 μsec for a particular cycle, the Nios II code reads the wrong time and calculates an incorrect target position

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- The hypothesis is that the Nios II interrupt controller doesn’t do nested interrupts correctly

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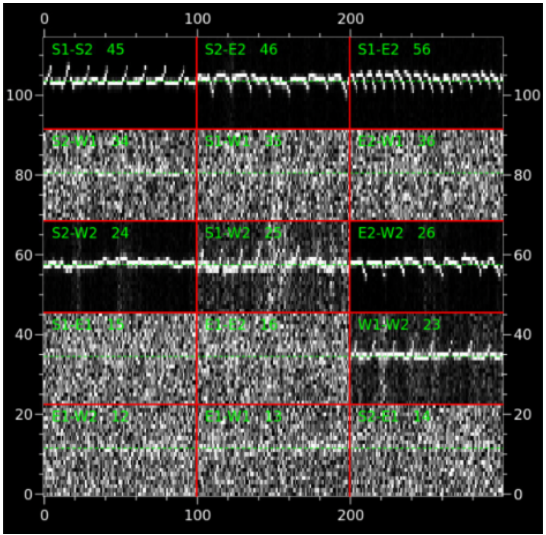
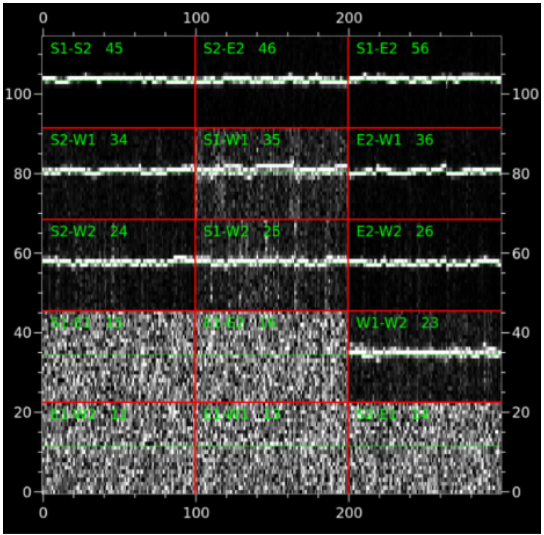

S1-S2 45
S2-E2 46
S1-E2 56
S2-W2 24
S1-W2 25
E2-W2 26
W1-W2 23
0
100
200
20
40
60
80

Future work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  - Logic still to be worked out

Thank You